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Claims

[c1] 1.A system for processing a logic function comprising a plurality of functional blocks each having output data, comprising:
(a)a first storage region;
(b)a second storage region;
(c)a reconfigurable logic array having defined therein a function region located outside said first and second storage regions; and
(d)a programmer in communication with said reconfigurable logic array and operatively configured to program said function region with ones of the plurality of functional blocks on a cyclical basis such that the output of successive ones of the plurality of functional blocks is stored in said first and second storage regions on an alternating basis.

[c2] 2.A system according to claim 1, wherein said first and second storage regions are located within said reconfigurable logic array, said programmer operatively configured to program said first and second storage regions.

[c3] 3.A system according to claim 2, wherein said function region includes a first edge and a second edge spaced

from said first edge, said first storage region located adjacent said first edge and said second storage region located adjacent said second edge.

[c4] 4.A system according to claim 1, further comprising a first fixed memory and a second fixed memory, said first storage region located within said first fixed memory and said second storage region located within said second fixed memory.

[c5] 5.A system according to claim 1, wherein said programmer is operatively configured to program said function region with ones of the plurality of functional blocks so that successive ones of the plurality of functional blocks process alternatingly in a first direction and a second direction substantially opposite said first direction.

[c6] 6.A system according to claim 5, wherein said function region includes a plurality of programmable logic elements having processing symmetry in said first and second directions.

[c7] 7.A system according to claim 1, wherein the system processes a plurality of functions simultaneously with one another, each of said plurality of functions having a plurality of functional blocks, said programmer operatively configured to program said reconfigurable logic

array with a functional block of each of the plurality of functions simultaneously with one another.

[c8] 8.A system according to claim 7, wherein said programmer programs said function region with a first functional block of a first one of the plurality of functions and a second functional block of a second one of the plurality of functions such that said first and second functional blocks process in opposite directions.

[c9] 9.A system according to claim 8, wherein said first and second functional blocks share first and second storage regions.

[c10] 10.A system according to claim 7, wherein said reconfigurable logic array contains a plurality of function regions each corresponding to a corresponding one of the plurality of functions.

[c11] 11.A system according to claim 10, wherein each of said plurality of function regions has a first edge and a second edge, said reconfigurable logic array including a plurality of storage regions each located adjacent a corresponding one of said first and second edges.

[c12] 12.A system according to claim 1, wherein said reconfigurable logic array includes a first function region and a second function region, said programmer operatively

configured to program said first and second function regions alternatingly with respect to one another.

[c13] 13.A reconfigurable logic array for processing a function, comprising:
(a)a plurality of programmable logic elements, at least some of said programmable logic elements configured with an Mth functional block of the function, said Mth functional block having output data and a first edge; and
(b)a first storage region located adjacent said first edge and containing said output data.

[c14] 14.A reconfigurable logic array of claim 13, wherein said Mth functional block has a second edge spaced from said first edge, the reconfigurable logic array further comprising a second storage region containing output data of an "M-1" functional block.

[c15] 15.A reconfigurable logic array of claim 13, wherein a first portion of said plurality of programmable logic elements is configured with a first functional block of a first function and a second portion of said plurality of programmable logic elements is configured with a second functional block of a second function.

[c16] 16.A reconfigurable logic array of claim 15, wherein said first functional block is configured for processing in a

first direction and said second functional block is configured for processing in a second direction opposite said first direction.

[c17] 17.A reconfigurable logic array of claim 15, wherein the reconfigurable logic array further comprises a first storage region corresponding to each one of said first and second functions.

[c18] 18.A reconfigurable logic array of claim 15, wherein said first and second functions share said first storage region.

[c19] 19.A reconfigurable logic array of claim 13, wherein a first portion of said plurality of programmable logic elements are configured with said Mth functional block of the function and a second portion of said plurality of programmable logic elements are configured with an "M+1"functional block of the function.

[c20] 20.A method of processing a function partitioned into a plurality of functional blocks, comprising the steps of:
(a)programming a reconfigurable logic array with a first one of the plurality of functional blocks so that said first one of the plurality of functional blocks processes in a first direction;
(b)processing said first one of the plurality of functional blocks in said first direction;

(c)programming said reconfigurable logic array with a second one of the plurality of functional blocks so that said second one of the plurality functional blocks processes in a second direction substantially opposite said first direction; and
(d)processing said second one of the plurality of functional blocks in said second direction.

[c21] 21.A method according to claim 20, wherein said reconfigurable logic array contains a function region and step (a) includes programming said function region and step (c) includes reprogramming said function region.

[c22] 22.A method according to claim 20, wherein said reconfigurable logic array contains a first function region and a second function region and step (a) includes programming said first function region and step (c) includes programming said second function region.

[c23] 23.A method according to claim 20, wherein said first one of the plurality of functional blocks has output data, the method further comprising, prior to step (b), the step of programming a first storage region within said reconfigurable logic array, said first storage region for containing said output data.

[c24] 24.A method according to claim 23, wherein said second

one of the plurality of functional blocks has output data, the method further comprising, prior to step (d), the step of programming a second storage region within said reconfigurable logic array for containing said output data of said second one of the plurality of functional blocks.

[c25] 25.A method according to claim 20, wherein steps (b) and (c) are performed simultaneously with one another.

[c26] 26.An integrated circuit chip, comprising:
(a)a system for processing a function partitioned into a plurality of functional blocks, comprising:
(i)a reconfigurable logic array; and
(ii)a programmer operatively configured to program said reconfigurable logic array with a first one of the plurality of functional blocks so that said first one of the plurality of functional blocks processes in a first direction and program said reconfigurable logic array with a second one of the plurality of functional blocks so that said second one of the plurality of functional blocks processes in a second direction substantially opposite said first direction.

[c27] 27.An integrated circuit chip according to claim 26, wherein said first one of the plurality of functional blocks has first output data and said second one of the plurality of functional blocks has second output data, said pro-

grammer operatively configured to program said reconfigurable logic array with a first storage region for storing said first output data and program said reconfigurable logic array with a second storage region for storing said second output data.

[c28] 28.An integrated circuit chip according to claim 26, wherein said reconfigurable logic array includes a plurality of programmable logic elements at least some of which are functionally symmetric in said first and second directions.

[c29] 29.An integrated circuit chip according to claim 26, wherein said reconfigurable logic array contains a function region, said programmer operatively configured to program said function region with ones of the plurality of functional blocks in serial succession with one another.

[c30] 30.An integrated circuit chip according to claim 29, wherein each successive pair of adjacent functional blocks process in opposite directions relative to said reconfigurable logic array.